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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,481	04/14/2004	Vaishnav Srinivas	030333	8117

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Qualcomm Incorporated
Patents Department
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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/825,481	SRINIVAS ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8,10-12,17-23 and 25-27 is/are rejected.

7)☒ Claim(s) 9,13-16 and 24 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 14 April 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Drawings

The informal drawings filed on 04/14/04 is accepted for examination purpose only.

Claim Objections

Claim 10 is objected to because of the following informalities:

In claim 10, last line, after "node", --, -- should be replaced with -- . -- .

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 8, it is unclear as to whether "input signal" recited in last line is additional limitation "an input signal" as previously cited in claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 8, 10-12, 17-23, 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Shirasaki (U.S Patent No. 6,587,100).

Regarding claim 1:

a driver (121, 132) configure to switch a current source and a current sink to a load (switch 121, 132); and

predriver (110, 141, 142, 143, 145, 146,) having first and second cross-coupled inverters (111, 112, 113 and 114) responsive to an input signal (output signal of 141), the first inverter (112, 113) being configured to control the switching of the current source to the load and the second inverter (111, 114) being configured to control the switching of the current sink to the load, wherein the cross-coupling between the first and second inverters (111-114) is configured such that the first inverter (112, 113) removes the current source from the load before the second inverter (111, 114) switches the current sink to the load in response to a transition in the input signal (the output signal of 141), and the second inverter (111, 114) removes the current sink from the load before the first inverter (112, 113) switches the current source to the load in response to an opposite transition in the input signal (via inverter 142) (depending on a rising edge, or a falling edge, i.e: the signal output is sent to output driver 121 or 132, when input signal is High, the following output signal applied to 121 provides a current sink for the load, when input signal is Low, the following output signal applied to 132 provides a current source for the load, due to different sizes and different delay, 121 switches faster than 132). Moreover, due to the claimed structure is fully met by Shirasaki, the function "control the switching of the current to the load ... switches the current source to the load in response to an opposite transition in the input signal" will necessarily be inherent in Shirasaki, as held by the court in In re Best, 195 USPQ 430)

Regarding claim 2: each of the inverters comprises a pair of transistors connected in series (112-114).

Regarding claim 3: each of the transistors comprises a field effect transistor (112-114).

Regarding claim 4: each of the inverters comprises a p-channel FET (111, 113) having a drain and an n-channel FET (112, 114) having a drain connected to the drain of the PFET (111, 113).

Regarding claim 5: each of the inverters (111-114), the NFET (112 or 114) comprises a gate responsive to the input signal (the output of 141), and the PFET (111 or 113) comprises a gate coupled to the drain of the PFET (113 or 111) in the other inverter.

Regarding claim 6: each of the inverters (111-114), the NFET (112, 114) is larger than the PFET (111, 113) (W/L of 112, 114 is 30/1 and W/L or 111, 113 is 3/30).

Regarding claim 7: the NFET (112) in the first inverter (112, 113) is substantially the same size (W/L = 30/1) as the NFET (114) in the second inverter (111, 114), and wherein the PFET (113) in the first inverter (112, 113) is substantially the same size (W/L = 3/30) as the PFET (111) in the second inverter (111, 114).

Regarding claim 8: Element VU0 reads on a voltage source coupled to the inverters (111-114), the voltage source VUO providing level shifting at an output of each inverter in response to the input signal (the output of 141).

Regarding claim 10:

an input inverter (142) configured to receive an input signal (output signal of 141);

two cross-coupled inverters (111-114) that include a first and second NFET (112, 114) and a first and second PFET (111, 113), wherein the first NFET (114) is configured to receive the output of the input inverter (142), and wherein the second NFET (112) is configured to receive the input signal (the output signal of 141);

first and second output buffers (first (143); second (145, 146)) configured to receive first and second outputs (at node N1, N2) of the two cross-coupled inverters (111-114); and

wherein the NFETs (112, 114) of the cross-coupled inverters are larger than the PFETs (111, 113) of the cross-coupled inverters (W/L of 112, 114 = 30/1, W/L of 111, 113 = 3/30), the NFETs (112, 114) and PFETs (111, 113) being sized (different size) with respect to each other such that a break before make delay is created (due to different W/L) between a first predriver output signal at a first predriver output node (N1) and a second predriver output signal at a second predriver output node (N2).

Regarding claim 11: due to different sizes of the input inverter (142, W/L: P10/1, N10/1), the cross coupled inverters (112, 114: W/L = 30/1), the first and second output buffers (W/L of 145 = P3/1, n3/1, W/L of 146 = P10/1, N5/1, and W/L of 143 = P3/1, N3/1), the function "first and second delays ... are substantially equal" and "third and fourth delays ... are substantially equal" is fully met.

Regarding claim 12: the PFETs of the cross-coupled inverters are substantially equal in size (W/L of 111, 113 = 3/30).

Regarding claim 17: an output driver device (121, 132) configured to receive the first and second predriver output signals (node N1, N2), the output driver device being further configured to drive a capacitive load (inherent seen in 120, 130).

Regarding claim 18: wherein each of the input inverter , the cross-coupled inverters and the first and second output buffers are further sized (W/L of 142 = P10/1, N10/1, W/L of 112, 114 = 30/1, W/L of 145 = P3/1, n3/1, W/L of 146 = P10/1, N5/1, and W/L of 143 = P3/1, N3/1),), so as to be sufficiently large to drive the capacitive load (due to different size).

Regarding claim 19: the output driver device includes an NFET device (132) and a PFET device (121).

Regarding claim 20: element VUO reads on a voltage supply.

Regarding claim 21: the voltage supply VUO is coupled between the first and second PFETs (111, 113) of the cross-coupled inverter.

Regarding claim 22: the output buffers include one or more inverters (143, 145, 146).

Claim 23 is similarly rejected as above claim 10: inverter means (142), cross-coupled inverter means (111-114) and first and second output buffer means (143; 145, 146).

Element VUO reads on voltage supply means as recited in claim 25.

Claims 26-27 are similarly rejected as claims above: i.e, an input signal (output signal of 141), two cross-coupled inverters (111-114) including a pair of NFETs (112,

114) and a pair of PFETs (111, 113), and first and second output buffers (143; 145, 146).

Claims 10-12, 11-23, 25-27 are also rejected under 35 U.S.C. 102(b) as being anticipated by Bismarck (U.S Patent No. 4,450,371).

Regarding claim 10:

an input inverter (I1) configured to receive an input signal (IN);

two cross-coupled inverters (P1, P2, N1, N2) that include a first and second NFET (N1, N2) and a first and second PFET (P1, P2), wherein the first NFET (N1) is configured to receive the output of the input inverter (IN*), and wherein the second NFET (N2) is configured to receive the input signal (IN);

first and second output buffers (I4, I5) configured to receive first and second outputs (20, 22) of the two cross-coupled inverters (P1, P2, N1, N2); and

wherein the NFETs (N1, N2) of the cross-coupled inverters are larger (inherent seen in see col. 3, line 16-19: P1 or P2 is smaller than N1 or N2 due to the ON impedance of P1, P2 is much larger than the ON impedance of N1 or N2) than the PFETs (P1, P2) of the cross-coupled inverters, the NFETs (N1, N2) and PFETs (P1, P2) being sized (different size) with respect to each other such that a break before make delay is created (due to different W/L) between a first predriver output signal at a first predriver output node (20) and a second predriver output signal at a second predriver output node (22).

The limitation recited in claim 11 is inherent seen in col. 3, line 16-col. 5, line 5.

Regarding claim 12: the PFETs (P1, P2) of the cross-coupled inverters are substantially equal in size (both SMALL in size).

Regarding claim 20: element VDD reads on a voltage supply.

Regarding claim 21: the voltage supply VDD is coupled between the first and second PFETs (P1, P2) of the cross-coupled inverter.

Regarding claim 22: the output buffers include one or more inverters (I4, I5).

Claim 23 is similarly rejected as above claim 10: inverter means (I1), cross-coupled inverter means (P1, P2, N1, N2) and first and second output buffer means (I4, I5).

Element VDD reads on voltage supply means as recited in claim 25.

Claims 26-27 are similarly rejected as claims above: i.e, an input signal (IN), two cross-coupled inverters (P1, P2, N1, N2) including a pair of NFETs (N1, N2) and a pair of PFETs (P1, P2), and first and second output buffers (I4, I5).

.Allowable Subject Matter

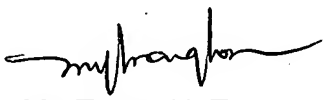
Claims 9, 13-16, 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "the inverters ... from the load concurrently to allow tristate" as recited in claim 9; "first and second tristate devices configured to disable the output signals of the first and second predriver output nodes" as recited in claim 13; "first and

second tristate means for disabling the output signals of the first and second predriver output nodes" as recited in claim 24.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

May 9, 2005